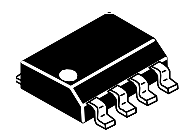
33290

ISO K Line Serial Link Interface

The 33290 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller and systems off-board the vehicle via the special ISO K line. The 33290 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and overtemperature conditions.

The 33290 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the 33290 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of $-40°C \leq T_A \leq 125°C$ and $8.0\ V \leq V_{BB} \leq 18\ V$ supply. The economical SO-8 surface-mount plastic package makes the 33290 very cost effective.

ISO K LINE SERIAL LINK INTERFACE



D SUFFIX
PLASTIC PACKAGE
CASE 751
(8-SOICN)

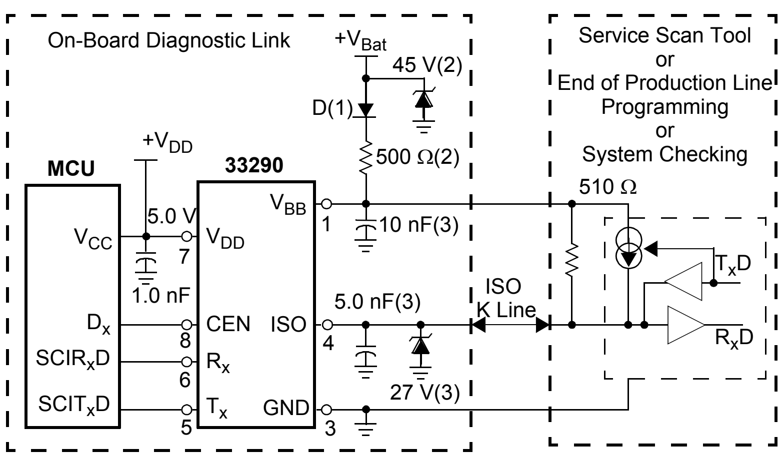
Features

- Designed to Operate Over Wide Supply Voltage of 8.0 to 18 V
- Ambient Operating Temperature of -40 to 125°C
- Interfaces Directly to Standard CMOS Microprocessors
- ISO K Line Pin Protected Against Shorts to Ground
- Thermal Shutdown with Hysteresis
- ISO K Line Pin Capable of High Currents
- ISO K Line Can Be Driven with up to 10 nF of Parasitic Capacitance
- 8.0 kV ESD Protection Attainable with Few Additional Components
- Standby Mode: No V_{Bat} Current Drain with V_{DD} at 5.0 V
- Low Current Drain During Operation with V_{DD} at 5.0 V

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33290D/DR2	-40 to 125°C	8-SOICN

33290 Simplified Application Diagram



Components necessary for Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case. This device contains 85 active transistors.

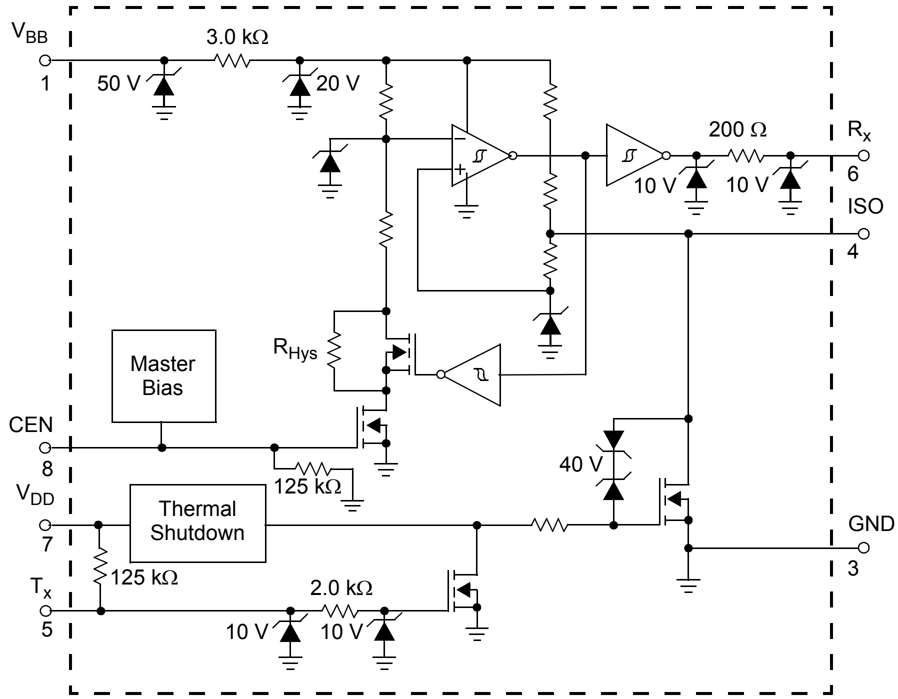
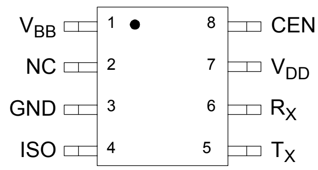


Figure 1. 33290 Simplified Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	V_{BB}	Battery power through external resistor and diode.
2	NC	Not to be connected. (Note 1)
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	T_X	Logic level input for data to be transmitted on the bus.
6	R_X	Logic output of data received on the bus.
7	V_{DD}	Logic power source input.
8	CEN	Chip enable. Logic “1” for active state. Logic “0” for sleep state.

Notes
1. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
V_{DD} DC Supply Voltage	V_{DD}	-0.3 to 7.0	V
V_{BB} Load Dump Peak Voltage	$V_{BB(LD)}$	45	V
ISO Pin Load Dump Peak Voltage (Note 2)	V_{ISO}	40	V
ISO Short Circuit Current Limit	$I_{ISO(LIM)}$	1.0	A
ESD Voltage (Note 3) Human Body Model (Note 4) Machine Model (Note 5)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
ISO Clamp Energy (Note 6)	E_{clamp}	10	mJ
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Case Temperature	T_C	-40 to +125	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Power Dissipation T_A = 25°C	P_D	 0.8	W
Lead Soldering Temperature (Note 7)	T_{solder}	260	°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	 150	°C/W

Notes

2. Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
3. ESD data available upon request.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. Nonrepetitive clamping capability at 25°C.
7. Lead soldering temperature limit is for 10 seconds maximum duration. Contact the Motorola Sales Office for device immersion soldering time/ temperature limits.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V_{DD} Sleep State Current T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{DD(SS)}$	–	–	0.1	mA
V_{DD} Quiescent Operating Current T_x = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{DD(Q)}$	–	–	1.0	mA
V_{BB} Sleep State Current V_{BB} = 16 V, T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{BB(SS)}$	–	–	50	µA
V_{BB} Quiescent Operating Current T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High-Voltage Threshold (Note 8) Input Low-Voltage Threshold (Note 9)	 $V_{IH(CEN)}$ $V_{IL(CEN)}$	 0.7 V_{DD} –	 – –	 – 0.3 V_{DD}	V
Chip Enable Pull-Down Current (Note 10)	$I_{PD(CEN)}$	2.0	–	40	µA
T_X Input Low-Voltage Threshold R_{ISO} = 510 Ω (Note 11)	$V_{IL(Tx)}$	–	–	0.3 x V_{DD}	V
T_X Input High-Voltage Threshold R_{ISO} = 510 Ω (Note 12)	$V_{IH(Tx)}$	0.7 x V_{DD}	–	–	V
T_X Pull-Up Current (Note 13)	$I_{PU(Tx)}$	-40	–	-2.0	µA
R_X Output Low-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}, R_x Sinking 1.0 mA	$V_{OL(Rx)}$	–	–	0.2 V_{DD}	V
R_X Output High-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}, R_X Sourcing 250 µA	$V_{OH(Rx)}$	0.8 V_{DD}	–	–	V
Thermal Shutdown (Note 14)	T_{LIM}	150	170	–	°C

Notes

8. When IBB transitions to >100 µA.
9. When IBB transitions to <100 µA.
10. Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at 0.3 V_{DD}.
11. Measured by ramping T_X down from 0.7 V_{DD} and noting T_X value at which ISO falls below 0.2 V_{BB}.
12. Measured by ramping T_X up from 0.3 V_{DD} and noting the value at which ISO rises above 0.9 V_{BB}.
13. T_x pin has internal current pull-up. Pull-up current is measured with T_X pin at 0.7 V_{DD}.
14. Thermal Shutdown performance (T_{LIM}) is guaranteed by design but not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
Input Low Voltage Threshold R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} (Note 15)	$V_{IL(ISO)}$	–	–	0.4 x V_{BB}	V
Input High Voltage Threshold R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} (Note 16)	$V_{IH(ISO)}$	0.7 x V_{BB}	–	–	V
Input Hysteresis (Note 17)	$V_{Hys(ISO)}$	0.05 x V_{BB}	–	0.1 x V_{BB}	V
Internal Pull-Up Current R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}, V_{ISO} = 9.0 V, V_{BB} = 18 V	$I_{PU(ISO)}$	-5.0	–	-140	µA
Short Circuit Current Limit (Note 18) R_{ISO} = 0 Ω, T_X = 0.4 V_{DD}, V_{ISO} = V_{BB}	$I_{SC(ISO)}$	50	–	1000	mA
Output Low Voltage R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}	$V_{OL(ISO)}$	–	–	0.1 x V_{BB}	V
Output High Voltage R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}	$V_{OH(ISO)}$	0.95 x V_{BB}	–	–	V

Notes

15. ISO ramped from 0.8 V_{BB} to 0.4 V_{BB}, Monitor R_X, Value of ISO voltage at which R_X transitions to 0.3 V_{DD}.
16. ISO ramped from 0.4 V_{BB} to 0.8 V_{BB}, Monitor R_X, Value of ISO voltage at which R_X transitions to 0.7 V_{DD}.
17. Input Hysteresis, $V_{Hys(ISO)} = V_{IH(ISO)} - V_{IL(ISO)}$.
18. ISO has internal current limiting.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time (Note 19)	$t_{fall(ISO)}$				μs
R_{ISO} = 510 Ω to V_{BB}, C_{ISO} = 10 nF to Ground		–	–	2.0	
ISO Propagation Delay (Note 20)	$t_{PD(ISO)}$				μs
High to Low: R_{ISO} = 510 Ω, C_{ISO} = 500 pF (Note 21)		–	–	2.0	
Low to High: R_{ISO} = 510 Ω, C_{ISO} = 500 pF (Note 22)		–	–	2.0	

Notes

19. Time required ISO voltage to transition from 0.8 V_{BB} to 0.2 V_{BB}.
20. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
21. Step T_X voltage from 0.2 V_{DD} to 0.8 V_{DD}. Time measured from $V_{IH(ISO)}$ until V_{ISO} reaches 0.3 V_{BB}.
22. Step T_X voltage from 0.8 V_{DD} to 0.2 V_{DD}. Time measured from $V_{IL(ISO)}$ until V_{ISO} reaches 0.7 V_{BB}.

Electrical Performance Curves

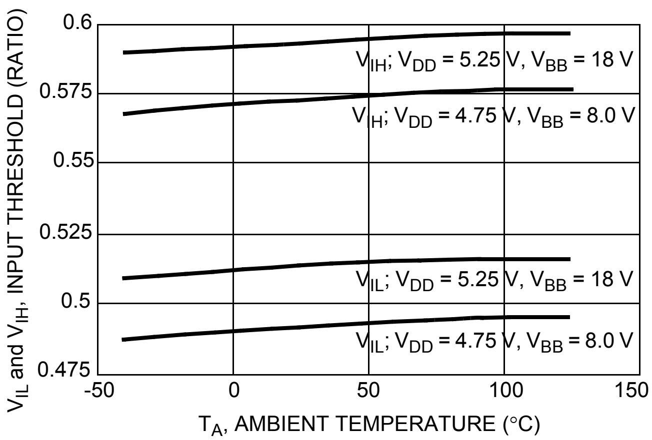


Figure 2. ISO Input Threshold/V_{BB} vs. Temperature

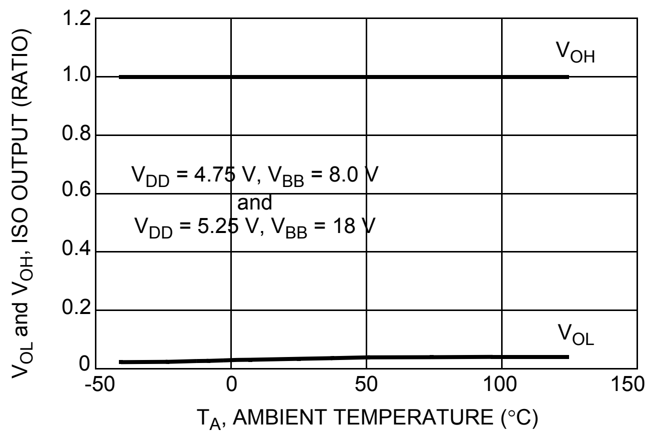


Figure 4. ISO Fall Time vs. Temperature

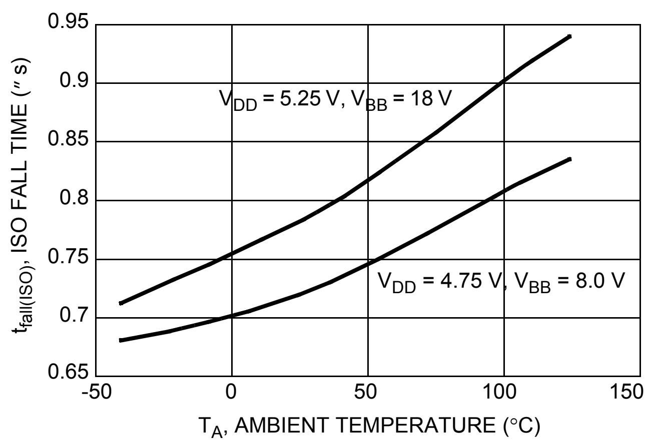


Figure 3. ISO Output/V_{BB} vs. Temperature

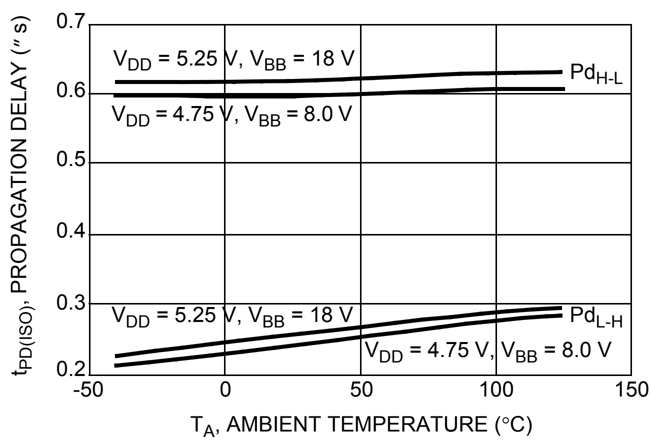


Figure 5. ISO Propagation Delay vs. Temperature

APPLICATIONS INFORMATION

INTRODUCTION

The 33290 is a serial link bus interface device conforming to the ISO 9141 physical bus specification. The device was designed for automotive environment usage compliant with On-Board Diagnostic (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line. The device does not incorporate an ISO L line. It provides bi-directional half-duplex communications interfacing from a microcontroller to the communication bus. The 33290 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic and from battery level logic to 5.0 V logic levels. The 33290 is built using Motorola's SMARTMOS process and is packaged in an 8-pin plastic SOIC.

FUNCTIONAL DESCRIPTION

The 33290 transforms 5.0 V microcontroller logic signals to battery level logic signals and visa versa. The maximum data rate is set by the fall time and the rise time. The fall time is set by the output driver. The rise time is set by the bus capacitance and the pull-up resistors on the bus. The fall time of the 33290 allows data rates up to 150 kbps using a 30 percent maximum bit time transition value. The serial link interface will remain fully functional over a battery voltage range of 6.0 to 18 V. The device is parametrically specified over a dynamic V_{BB} voltage range of 8.0 to 18 V.

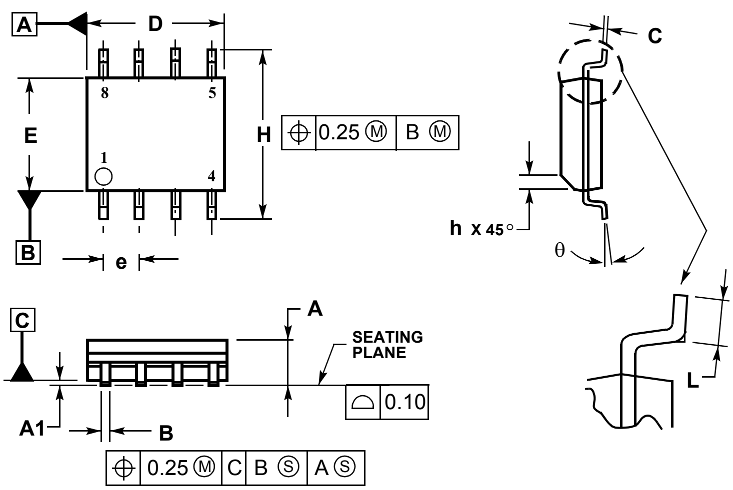
Required input levels from the microcontroller are ratio-metric with the V_{DD} voltage normally used to power the microcontroller. This enhances the 33290's ability to remain in harmony with the R_X and T_X control input signals of the microcontroller. The R_X and T_X control inputs are compatible with standard 5.0 V CMOS circuitry. For fault-tolerant purposes the T_X input from the microcontroller has an internal passive pull-up to V_{DD}, while the CEN input has an internal passive pull-down to ground.

A pull-up to battery is internally provided as well as an active data pull-down. The internal active pull-down is current-limit-protected against shorts to battery and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external 510 Ω pull-up resistor and diode to battery.

Reverse battery protection of the device is provided by using a reverse battery blocking diode ("D" in the Simplified Application Diagram on page 1). Battery line transient protection of the device is provided for by using a 45 V zener and a 500 Ω resistor connected to the V_{BB} source as shown in the same diagram. Device ESD protection from the communication lines exiting the module is through the use of the capacitor connected to the V_{BB} device pin and the capacitor used in conjunction with the 27 V zener connected to the ISO pin.

PACKAGE DIMENSIONS

D SUFFIX
(8-LEAD SOIC)
PLASTIC PACKAGE
CASE 751-06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

NOTES

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:
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